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TOPOLOGY FOR A DSP BASED BEAM CONTROL SYSTEM IN THE AGS BOOSTER*

J. DeLong, J.M. Brennan, T. Hayes, Tuong N. Le, K. Smith
Brookhaven National Laboratory, Upton N.Y. 11973

*Abstract**

The AGS Booster supports beams of ions and protons with a wide range of energies on a pulse-by-pulse modulation basis. This requires an agile beam control system highly integrated with its controls. To implement this system digital techniques in the form of: Digital Signal Processors, Direct Digital Synthesizers, digital receivers and high speed Analog to Digital Converters are used. Signals from the beam and cavity pick-ups, as well as measurements of magnetic field strength in the ring dipoles are processed in real time. To facilitate this a multi-processor topology with high bandwidth data links is being designed.

1 SYSTEM OVERVIEW

The AGS Booster acceleration system consists of two pairs of RF cavities with two frequency bands. The first group of cavities has a bandwidth of 2.5MHz and is capable of providing 45kV per station, the second group has a wider bandwidth of 5.5MHz and each cavity can provide up to 17kV [1].

To use these systems effectively the voltage and frequency of each individual accelerating station must be changed dynamically. Different ion species require very different acceleration cycles and bunch manipulations such as merging, rotating and squeezing require the low level RF drive system to be fast and flexible. This speed and flexibility is realized by using DSP controlled direct digital synthesizers with frequency, phase and amplitude modulation.

The beam control system must calculate the revolution frequency of the beam in real time as a function of dipole field and radial steering. This frequency program is corrected by feedback from measurements of the beam phase and radial position. The beam position and phase are measured using digital receiver technology [2]. The beam control system will also synchronize the Booster and the AGS to enable bunch to bucket transfer of beam between the two machines.

2 DSP TOPOLOGY

To accomplish all the required tasks in real time it is necessary to divide the problem into smaller pieces, the block diagram in figure 2 shows how the tasks are split among five Analog Devices ADSP-21160 DSP processors and how each task communicates with the others.

Data transfer between DSPs use the six available Link Ports [3] on each processor. The link ports are bi-directional byte serial communication ports that run at the 80 MHz core clock speed of the DSP. All data in the system is 32 bits wide and each port can transfer 80MB per second. The architecture of the DSP allows all six ports to run at this rate simultaneously without impacting the core process. This high-speed data IO architecture in addition to the 64bit global bus was the primary reason for choosing this DSP.

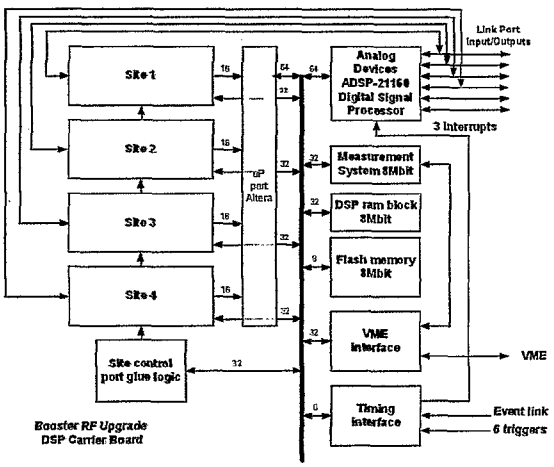

FIGURE 1. DSP carrier board block diagram.

To effectively utilize the capabilities of the DSP processor a carrier card has been designed (FIGURE 1). This printed circuit uses the VME bus form factor with a 32bit VME slave interface. Each carrier card can hold up to four peripheral devices such as digital synthesizers or analog to digital converters. Each peripheral has access to the DSP global bus and one link port as well as power supplies and flexible digital control signals. The DSP boots from an on board flash memory and the carrier also provides 4MB of zero wait state static RAM. Three field programmable gate arrays that are connected to the DSP global bus and each of the four peripheral sites further enhance this flexibility.

The DSP carrier board VME slave interface includes interrupter capability. This allows for tight integration into the control system. The host processor, a Motorola Power PC running the VxWorks operating system, has access to the internal memory space of the DSP as well as control of the peripherals and on board SRAM. Storing user specific program data in local memory and changing a pointer when the context of the machine changes can easily implement pulse-by-pulse modulation or changing of operating parameters of the machine on a system event.

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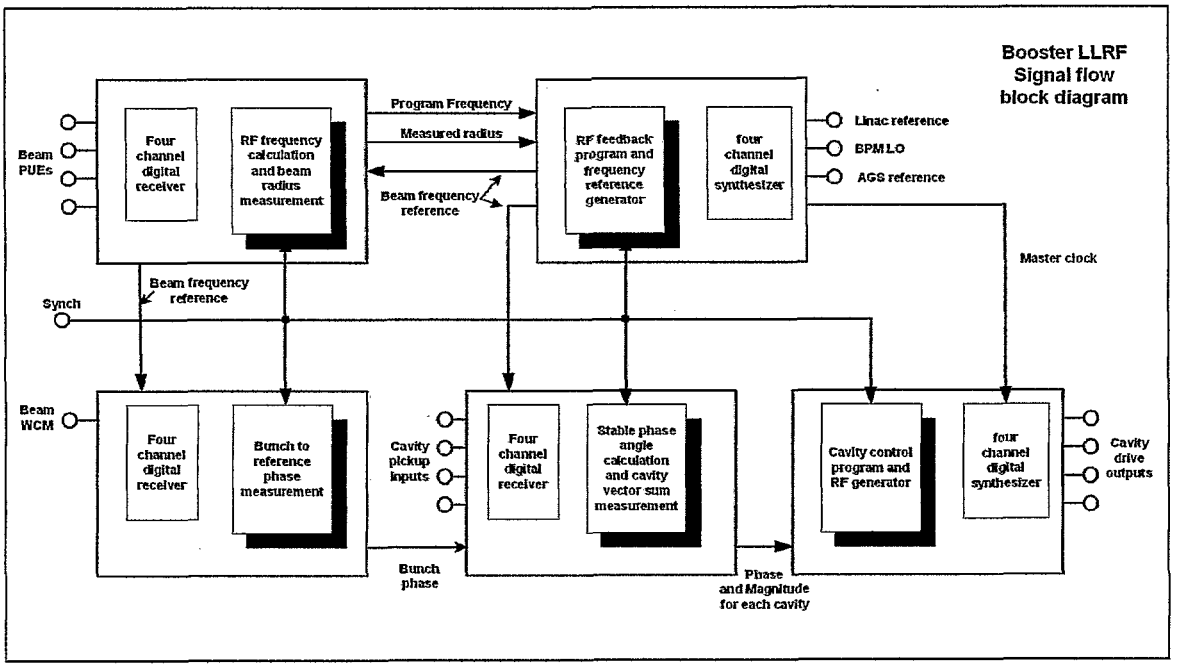

figure 2. shows the general layout of the RF system as well as the programming tasks and interprocessor communication paths.

3 SYSTEM PROGRAMMING TASKS

As shown in figure 2 the programming tasks are divided among the five processors. Each task is synchronized with an external strobe that executes an interrupt service routine on the DSP. This synchronization ensures that all calculations across the system processors are using the most current data.

3.1 Frequency program

The revolution frequency of the beam is calculated at a rate of 500kHz. This rate is sufficient to ensure frequency steps that are small compared to the RF bucket height. A memory-mapped accumulator on the DSP carrier board integrates the Gauss Clock (B train) and a radial steering function downloaded into local memory provide the two dynamic independent variables for this calculation. The control software calculates an acceleration parameter based on the mass and charge of the ion to be accelerated and stores this constant in DSP memory. The result of this calculation is passed to the feedback program via a link port.

3.2 Phase measurement

The bunch to bucket phase is the result of two separate measurements. The wall current signal from the ring is digitized and translated to DC by a digital receiver. The frequency translation is maintained at DC by the feedback program, which provides the Local Oscillator frequency. The phase measured by this receiver is compared to that measured by a four channel receiver connected to the Booster accelerating cavities. This receiver measures the vector sum of the cavities. As shown in FIGURE 3 the difference is sampled by the DSP. Phase offsets to compensate for the stable phase angle and cable lengths are added by the DSP and a phase error signal in transmitted to the feedback DSP using a link-port.

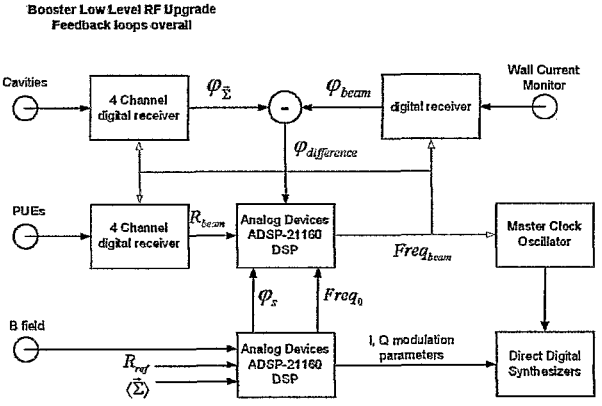

FIGURE 3. Phase loop signal flow diagram.

3.3 Radial position measurement

The radial position of the beam is measured using a four channel digital receiver. The positions at two points in the ring, 180 degrees apart in betatron phase, are averaged to remove any errors caused by distortions in the beam orbit. The signals from the PUEs are digitized and translated to base-band the normalized difference in magnitude between the two plates in the horizontal plane are calculated. This radial signal it transmitted to the feedback DSP using a link-port.

3.4 feedback program

The feedback program calculates the beam frequency from data received from the program and vector sum DSPs. The phase loop damps coherent synchrotron oscillations while the radial loop maintains the horizontal position of the beam according to a programmed function. The radial position measurement and calculated frequency are received from the program DSP and the bunch to bucket phase from the vector sum DSP. The integral of the radial error is calculated locally and is summed with the phase and radial errors. The instantaneous frequency of the beam is the sum of the error terms and the frequency program.

3.5 cavity voltage feedback

The four ferrite loaded cavities in the Booster ring require dynamic tuning to stay on resonance during the acceleration cycle. Imperfections in this tuning as well as characteristics of the amplifier chain require an automatic gain control circuit to flatten the response. To realize this in the LLRF drive chain the voltage of each cavity is measured in the vector sum DSP and compared to a command function downloaded into its local memory. The amplitude of that station's synthesizer is modulated to compensate for errors detected at the cavity.

3.6 synchronization

Synchronization for extraction is implemented in the feedback DSP. The Booster beam is extracted without a flattop, requiring synchronization while the frequency in the booster is still changing. To implement this we will take advantage of the repeatability of the Booster dipole field. The beam frequency, as applied to the master oscillator, during first Booster pulse will be recorded in memory. The total phase accumulated in this cycle will be calculated and subsequent pulses in an AGS fill will be forced to accumulate the same amount of phase, plus the amount required to move to the next AGS bucket. A synchro loop will be imposed to lock the beam to the recorded table. Extraction will occur when the table reaches the correct phase.

4 DSP MEASUREMENT SYSTEM

One of the most difficult tasks in designing a digital beam control system is building in a measurement system capable of both verifying system operation and debugging problems. Data transfer from the target hardware to the control system client is slow compared to the Booster repetition frequency. To allow for this slow transfer, system memory on the DSP carrier board has dual port access. The DSP can write data to the RAM and the front-end computer can read that data without impacting the operation of the DSP.

In addition to the measurement system RAM an FPGA dedicated to timing tasks is implemented on the carrier. Timing information for the Booster is distributed on a serial data link. The data link is decoded in the FPGA and selected events will cause interrupts to the DSP. Each event is associated with a case statement in the software and is used to trigger different processes in the DSP including triggering measurements.

4 CONTROLS INTEGRATION

The Booster RF upgrade will take advantage of the tools built for RHIC. A rapid application development environment was designed for RHIC that gives non-expert programmers the ability to quickly design applications and control hardware under development. These programs running on the front-end computer interface with client applications running on workstations throughout the complex.

The Booster RF application will manage the pulse-by-pulse modulation of the machine. Functions such as radial steering and voltage command functions can be edited and downloaded to hardware from this application. The measurement system can be controlled by this software, triggering can be manipulated and most variables in the DSP code can be queried. Waveforms from the remote system can be processed and displayed by the application reducing the load on the real time system.

Managing the DSP code will also be done within the application. Code can be downloaded into flash from the application and the DSP can be rebooted remotely.

5. CONCLUSIONS

Many of the building blocks for this system are currently being tested. Prototypes of the DSP carrier board, digital receiver and DDS are now being evaluated. Preliminary results are very promising.

The interconnection of multiple processors using high-speed data links has been successful in the Brookhaven Relativistic Heavy Ion Collider. The Booster upgrade leverages many of the techniques learned in the design and operation of RHIC [4].

The use of digital receivers and improvements to digital synthesizers in the booster design will enhance the flexibility and reliability of this machine.

6. REFERENCES

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